A Template for Straight Forward Fabrication of Single Nanowire Devices

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There is high demand for easy and effective ways of manufacturing single NW devices both for fundamental research and for technology development of advanced electronic, electro-mechanical, optoelectronic and chemical devices. While useful information and devices can be obtained by studying NW *arrays*, some of the physics and performance associated with a *single* NW is lost due to averaging effects. We present a simple method of fabricating single NW devices. The devices were then directly used to make white light sensing, gas sensing and electrical measurements or the single nanowire device.

To fabricate single NW FETs, we begin with a p-type Si oxide substrate with a 500 nm SiO_2 top layer. Next, standard photolithographic techniques are used to pattern multiple 1 cm × 1 cm arrays of 100 µm x 100 µm squares with 5 µm spacing between each square. Using an e-beam evaporator, 200 nm thick Ag islands are formed with a 10 nm intermediate Cr layer for adhesion. Next, CuO NWs are grown by direct oxidation of copper (Figure 1). To remove the NWs cleanly from the surface without removing the intermediate amorphous oxide layer a 5 mm x 5 mm piece of PDMS is gently used to shear off the NWs (Figure 2.). The PDMS with high density NWs on the surface is placed in ethanol and ultrasonicated for 5min. Next, the NWs now dispersed in ethanol are deposited onto the electrode grids. Alternatively, the PDMS with a high density of NWs on the surface can directly be used to perform optical measurements of the NW array.

A high resolution optical microscope (500x to 1000x) is then used to locate a NW that bridges two of the Ag islands, and their location is recorded (electrode column and row number). Fig. 3(b) is an optical image of a single NW, bridging two small Ag electrodes. The two electrodes in contact with a single NW then operate as the source and the drain with the underlying silicon substrate as the back gate (Figure 4). To improve the ohmic contact a top electrode layer is deposited using standard photolithography techniques. The devices are then conveniently packaged into a proto-chip by wire bonding for subsequent gas and light sensing measurement

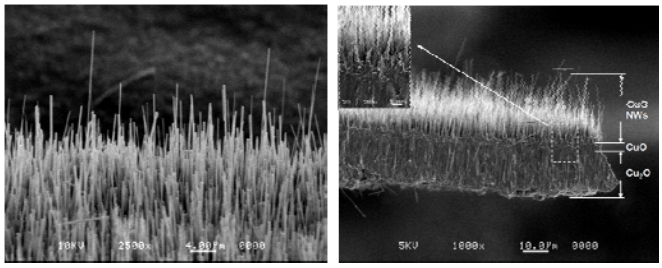

Figure 1: CuO nanowires grown by direct oxidation of copper at 500C for 150min in 100% O_2.

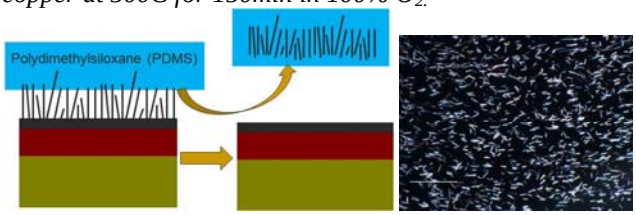

Figure 2: Clean Removal of CuO NWs using PDMS

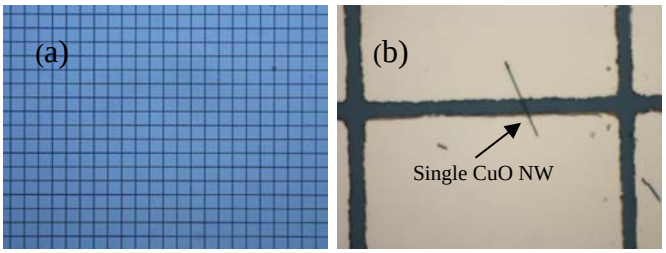

Figure 2. (a) Ag electrode grids (b) and single NW bridging two electrodes.

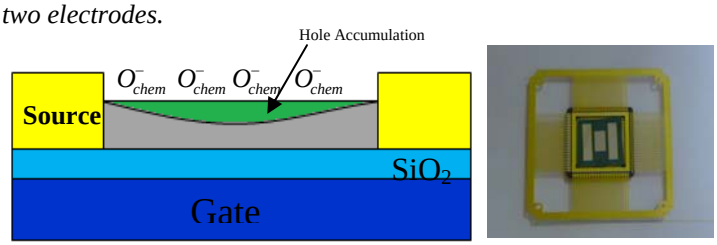

Figure 3. Schematic of Single NW device configuration and Device packaged into a functional proto-chip.