Heterogeneous Integration of Single-Walled Carbon Nanotubes with CMOS Circuitry

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Presentation

Short Description: **The integration of Single-Walled Carbon Nanotubes (SWNTs) with CMOS circuitry as a first step toward realizing highly sensitive nanosystems has been demonstrated. The realization of the integration of SWNTs onto CMOS circuitry is based on low temperature Dielectrophoresis (DEP) assembly process. Thermal response of SWNTs onto CMOS circuitry has further demonstrated which shows that the integrated nano devices can be used for sensing applications. This technique is simple, versatile and has a high yield where potential applications include the realization of nanotube and nanowire based nanosystems.**

Keywords: Carbon Nanotubes, CMOS integration.

Abstract: Despite the advances in nanowire and nanotube based sensors, system level approaches to nanotechnology is at its infancy. Carbon nanotubes, one of the prominent building blocks of nanotechnology, hold great promise as nanosensors due to their miniscule size, large surface area to volume ratio and extraordinary electrical and mechanical properties. Furthermore, due to their high sensitivity, their discrete implementation as sensors pose numerous challenges such as signal interference from the environment and/or noise along the signal paths demanding integration with on-chip CMOS circuitry. Depending on the application, integration with CMOS circuitry can provide high performance due to lower parasitic and reduced interconnect lines as well as the ability to provide signal conditioning and storage on the same chip [1].

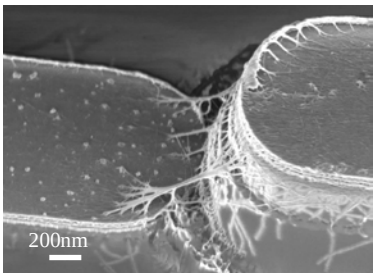

Fig.1 SWNTs integrated on CMOS circuitry

The CMOS chip comprising of the microelectrodes for the SWNT assembly and the interface circuitry was designed and fabricated using the AMI 0.5 µm CMOS process, provided by MOSIS. After receiving the fabricated chips, we first etched the oxide layer (Al2O3) on top of the Al metal electrodes and then coated them with a Zn layer using an electroless plating process [2]. Next, we deposit a 2-3 µl droplet of an aqueous solution containing the nanotubes on to the microelectrodes. An AC voltage of 5Vpp with a frequency of 10 MHz was utilized during the DEP assembly.

The SEM micrograph (Figure 1) shows the SWNTs assembled on to the microelectrodes. The I-V measurements from the assembled SWNTs displayed a resistance of ~22K ohms. The op-amp circuitry in the inverting configuration is utilized to demonstrate the integration of CNTs with CMOS electronics. A high gain op-amp circuitry was designed to demonstrate the integration of nanotubes with CMOS electronics. The SWNTs are into the feedback resistor of the op-amp. The small signal gain of the op-amp with CNT feedback resistors was measured as ~-1.95. The thermal response of SWNTs have been measured and has a negative temperature coefficient of resistance (TCR) ~ -0.4%. In summary, we have successfully integrated SWNTs on to functional CMOS circuitry utilizing a low temperature wafer scale process. The technique is simple, versatile and high yield with potential applications for the realization of nanotube and nanowire based bio and chemical sensors.

References

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